Exhibit A-12

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Expedited Procedure
Examining Group 1107
37 CFR 1.116

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	
James G. Gay et al.	:	
Serial No.: 08/145,117	:	Date: May 18, 1995
Filed: November 03, 1993	:	
For: A Data Processing System and Method	:	Group Art Unit: 2305
for Performing Dynamic Bus	:	Examiner: J. Seto
Termination	:	Docket No.: SC-02086A

5/25/95 JS

#6/B (A.E.) LDJ 5-25-95 entered LDJ 7-26-95

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS WASHINGTON, D.C. 20231, ON: 5-19-95

MOTOROLA INC

Kristen J. Herzog 5-19-95
SIGNATURE DATE

AMENDMENT UNDER 37 CFR 1.116

HONORABLE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SIR:

In timely response to an recently mailed final rejection, Applicants request reconsideration of the above-identified application in view of the amendments and remarks presented below. Please amend the application as follows:

IN THE CLAIMS:

2. (Amended) The data processing system of claim 1 wherein the circuitry for signal termination reduces

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signal reflection of a voltage signal input from the [at least one external pin] plurality of external pins when the enable signal is asserted.

5. (Amended) The data processing system of claim 1 wherein the enable signal is a function of a first control signal internal to the communication device and a second control signal internal to the device, the first control signal being asserted by the communication device if the communication device is functioning as a bus master and being deasserted if the communication device is functioning as a bus slave, the second control signal being in a first logic state if a read operation is occurring through the [at least one external pin] plurality of external pins and being in a second logic state if a write operation is occurring through the [at least one external pin] plurality of external pins.

26. (Twice Amended) The integrated circuit of claim 22 wherein each of the N physically separated termination circuits are enabled at any time to provide one of a number of different termination circuit combinations wherein the different circuit combinations are equal a number selected within the range of two to 2^N different termination circuit combinations, the one of a number of different termination circuit combinations being coupled to the terminal for communicating the [at] parallel binary data.

28. (Amended) An integrated circuit comprising:
circuitry for performing a predetermined function;
an external terminal of the integrated circuit for receiving data from external to the integrated circuit; and

bus termination circuitry coupled between the circuitry for providing a predetermined function and the external terminal, the bus termination circuitry providing a selected impedance to the external terminal in response to at least one control signal where the selected impedance is maintained for a time period while the external terminal is receiving the data, the bus termination circuitry being capable of providing a plurality of possible impedances to the external terminal in response to the at least one control signal, the impedances being provided via a plurality of resistive elements within the bus termination circuitry wherein at least two resistive elements are coupled to the external terminal by the termination circuitry in order to provide the selected impedance.

~~29~~ 28. (Amended) A method for providing a selected impedance to a plurality of terminals of an integrated circuit, the method comprising the steps of:

determining an optimal impedance required for the plurality of terminals;

communicating at least one control signal to circuitry coupled to the plurality of terminals, the at least one control signal comprising at least one read/write signal that indicates when the integrated circuit is being subject to a read or write operation; and

providing an impedance from an output of the circuitry to the plurality of terminals wherein the impedance provided by the circuitry is the optimal impedance, the optimal impedance being one impedance among a plurality of possible impedances where each possible impedance is capable of being provided by

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the circuitry, the optimal impedance being selected via the at least one control signal.

Remarks

In an Office Action mailed January 24, 1994, the Examiner rejected claims 2, 5, and 26 under 35 U.S.C. 112, second paragraph, as being indefinite. Applicants have corrected these problems herein via the above amendments. Therefore, Applicants respectfully request that the rejection of claims 2, 5, and 26 be removed.

The Examiner also rejected claims 28 and 29 under 35 U.S.C. 103 as being unpatentable over McMahan in view of Gubisch. Applicants have amended claims 28 herein to recite (in accordance with one mode of operation of FIGs. 6-8) that more than one resistive element is coupled to the terminal at a given time. McMahan teaches that only one resistor 18 or 34 is coupled to the system at a time, and Gubisch teaches that via a switch 65 only one of a resistor R1 through Rn is coupled to the system at any one time. Therefore, Neither McMahan or Gubisch teach or suggest that multiple resistors are coupled to the terminal to achieve the desired resistance.

Applicants have amended claim 29 to recite that the control signal comprises a read/write signal in accordance with FIG. 1. Neither of McMahan or Gubisch teach or suggest the read/write control signal as a impedance selector for resistance termination of a conductor. Therefore, due to the amendments to claims 28 and 29, Applicants respectfully request that the Examiner allow all the claims 1-30 thereby rendering the entire application allowable.

Applicants acknowledge that this amendment (regarding claims 28 and 29) may not be entered as a matter of right, but is discretionary subject to the findings of the Examiner under MPEP 714.12 and 714.13. Applicants believe that the amendments to claims 28 and 29 herein do not raise new issues requiring a new search or

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new consideration by the Examiner since issues related to the above amendments to claim 29 were previously addressed by the Examiner in allowable claims 18 and 19 and similar issues related to the amendments to claim 28 were previously addressed by the Examiner in allowable claim 22. In addition, the amendments made to claim 28 and 29 require only a simple and cursory review by the Examiner. These amendments further the application to allowance by clearly overcoming the prior art, or at the very least place the application in a better form for possible appeal. Therefore, the entrance of this amendment in full should be considered by the Examiner since Applicants believe that MPEP 714.12 and 714.13 favor the entrance of this amendment in full even though the entrance is discretionary.

Believing to have responded to all of the issues raised by the Examiner, claim 1-30, as amended herein, are readily distinguishable over the art of record. Therefore, claims 1-30 are believed to be in condition for allowance, which action is earnestly solicited, thereby placing the application in condition for allowance.

Respectfully submitted,
James G. Gay et al.

Keith Witek
Agent for Applicants
Registration No. 37,475
Telephone No. (512) 505-8906